UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/739,758	12/20/2000	Takao Watanabe	HIT 2 482-06	7380

24956 7590 02/17/2004

MATTINGLY, STANGER & MALUR, P.C.
1800 DIAGONAL ROAD
SUITE 370
ALEXANDRIA, VA 22314

EXAMINER	
HIRL, JOSEPH P	

ART UNIT	PAPER NUMBER
2121	19

DATE MAILED: 02/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No. 09/739,758	Applicant(s) WATANABE ET AL.	
	Examiner Joseph P. Hirl	Art Unit 2121	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 30 January 2004 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☒ The period for reply expires *three* months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☐ The proposed amendment(s) will not be entered because:

   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);

   (b) ☐ they raise the issue of new matter (see Note below);

   (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.

4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☒ The a)☐ affidavit, b)☐ exhibit, or c)☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: *See Continuation Sheet*.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☒ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: _____.

   Claim(s) rejected: *25-37*.

   Claim(s) withdrawn from consideration: _____.

8. ☐ The drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9. ☒ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). *17*.

10. ☐ Other: _____

ANIL KHATRI
SUPERVISORY PATENT EXAMINER

Continuation of 5. does NOT place the application in condition for allowance because: the arguments are not persuasive. Notwithstanding such conclusion, the following points are appropriate.

1. The rejection of claims 25-27, 29, 33 34 and 36 under under 35 USC 112 first paragraph are withdrawn.

2. The objections to Figs 1-25 related to prior art are withdrawn.

3. The objection to the IDS is withdrawn. A completed IDS is attached.

4. Related to the arguments made in relation to claim rejections under 35 USC 102:

a. Modes and use of MOS transistor

To one of ordinary skill in the art, it would be generic to first execute a memory operation (sort of like writing something down on paper, taking notes) before one executes an arithmetic operation (adding the numbers previously noted). For sure, one cannot execute an arithmetic before one has something to operate on. Mashiko teaches a semiconductor neural network. To one of ordinary skill in the art, such a circuit will have to contain, among other things, input/output means, memory means and computational (arithmetic) means. As one knows from the art, there simply isn't any other way to perform the work. Stated explicitly or otherwise, logic dictates that Mashiko's art functions in anticipation of the modes of the inventor...albeit many other pieces of art do also.

With all due respect, and again, to one of ordinary skill in the art, the use of methal-oxide semiconductor (MOS) is generic with nothing new to be established by a source/drain path between the arithmetic unit and a power line...all circuits have power sources...active or passive. Mashiko also uses MOS devices in a similar fashion as noted Mashiko at Fig. 8 B.

b. Three busses

Mathematics and the sciences are founded on the discipline of logic. Violate logic and the system simply will not function. Since it is axiomatic that one would have to have something in memory before a logic function can be performed on it, it follows that Mashiko must have data in memory before any logic pertaining to such data can be performed. It further follows that Mashiko's memory and logic functions operate independently. The applicant admits that Mashiko has buses that link switching elements and random memory cells and random memory cells and I/O (applicant response dated July 10, 2003 at page 13), Mashiko also has the link between the logic circuit and I/O as stated in Mashiko at c 2, lines 57-67, Figs 4, 5. At Fig. 4, Bi is the output which is derived from a switching (logic) circuit and which would be latched in the output data register. Consequently, Mashiko has the equivalent of three data buses.

5. The Examiner welcomes further discussion with the inventor concerning the outstanding issues under 35 USC 102. Other amendments will be considered. If the applicant feels so disposed, further personal interviews can be arranged.